CLAIMS

What is claimed is:

1. A multiplexer having a first data input lead, a second data input lead, and a data output lead, the multiplexer structure comprising:

a plurality of series capacitor coupling (SCC) structures, each SCC structure having an input lead, a control lead, and an output lead, wherein the input lead is capacitively coupled to the output lead when the control lead is floating, and wherein the input lead is de-coupled from the output lead when the control lead is driven with a DC voltage, wherein the input lead of a first of the SCC structures is the first data input lead of the multiplexer, and wherein the input lead of a second of the SCC structures is the second data input lead of the multiplexer, and wherein the output lead of the first SCC structure is coupled to the output lead of the second SCC structure; and

an output latch having an input lead and an output lead, the input lead of the output latch being coupled to the output lead of the first SCC structure, the output lead of the output latch being the data output lead of the multiplexer.

2. The multiplexer of Claim 1, wherein the DC voltage is ground potential.

3. The multiplexer of Claim 1, further comprising;

a memory cell structure that stores one bit of digital information, the memory cell structure having a first output lead that is driven with the DC voltage by the memory cell structure when the bit has a first digital value, and wherein the first output lead is not driven by the memory cell structure when the bit has a second digital value, wherein the first output lead of the memory cell structure is coupled to the control lead of the first SCC structure.

4. The multiplexer of Claim 3, wherein the memory cell structure has a second output lead, wherein the second output lead is driven with the DC voltage by the memory cell structure when the bit has the second digital value, and wherein the second output lead is not driven by the memory cell structure when the bit has the second digital value, and wherein the second output lead of the memory cell structure is coupled to the control lead of the second SCC structure.

5. The multiplexer of Claim 1, wherein the output latch comprises an amplifier portion and a latch portion, the amplifier portion amplifying a signal present on the input lead of the output latch and outputting an amplified form of the signal to the latch portion.

6. The multiplexer of Claim 1, wherein each of the SCC structures comprises a first capacitor plate that extends in a first plane, a second capacitor plate that extends in a second plane parallel to the first plane, and a third capacitor plate that extends in a third plane parallel to the second plane, wherein the first capacitor plate is the input lead of the SCC structure, wherein the second capacitor plate is the control lead of the SCC structure, and wherein the third capacitor plate is the output lead of the SCC structure.

7. The multiplexer of Claim 6, further comprising:

a memory cell structure that stores one bit of digital information, the memory cell structure having a first output lead that is driven with the DC voltage by the memory cell structure when the bit has a first digital value, and wherein the first output lead is not driven by the memory cell structure when the bit has a second digital value, wherein the first output lead of the memory cell structure is coupled to the control lead of the first SCC structure, wherein the

memory cell structure has a second output lead, wherein the second output lead is driven with the DC voltage by the memory cell structure when the bit has the second digital value, and wherein the second output lead is not driven by the memory cell structure when the bit has the first digital value, and wherein the second output lead of the memory cell structure is coupled to the control lead of the second SCC structure.

8. The multiplexer of Claim 6, further comprising:

a first memory cell structure that stores one bit of digital information, the first memory cell structure having an output lead that is driven with the DC voltage by the first memory cell structure when the bit has a first digital value, and wherein the output lead is not driven by the first memory cell structure when the bit has a second digital value, wherein the output lead of the first memory cell structure is coupled to the control lead of the first SCC structure; and

a second memory cell structure that stores one bit of digital information, the second memory cell structure having an output lead that is driven with the DC voltage by the second memory cell structure when the bit has a first digital value, and wherein the output lead is not driven by the second memory cell structure when the bit has a second digital value, wherein the output lead of the second memory cell structure is coupled to the control lead of the second SCC structure.

9. The multiplexer of Claim 1, wherein the multiplexer is part of a programmable interconnect structure of a programmable logic device.

10. The multiplexer of Claim 1, wherein the multiplexer is part of a programmable interconnect structure of a field programmable gate array, and wherein which of the first and

second data input leads is coupled through the multiplexer to the data output lead is determined by a bit of configuration information stored on the field programmable gate array in a memory cell.

11. The multiplexer of Claim 1, wherein the multiplexer is a two-to-one multiplexer that is a part of a larger multiplexer, wherein the larger multiplexer includes SCC structures in addition to the first and second SCC structures that are part of the two-to-one multiplexer.

12. The multiplexer of Claim 11, wherein the larger multiplexer is an N-to-1 multiplexer having N data input leads, wherein which of the N data input leads is coupled to a data output lead of the N-to-1 multiplexer is determined by a plurality of bits A of control information, each of the bits of control information being stored in a separate memory cell, wherein 2 to the power A is equal to N.

13. A method, comprising:

using a plurality of series capacitor coupling (SCC) structures to capacitively couple a selected one of a plurality of data input leads to an intervening node such that a signal edge of a first digital signal on the selected data input lead is coupled onto the intervening node and such that a signal edge of a second digital signal on another of the data input leads is blocked from being coupled onto the intervening node; and

latching the signal edge of the first digital signal on the intervening node to generate a digital output signal, wherein the digital output signal is a delayed version of the first digital signal.

14. The method of Claim 13, wherein each of the SCC structures includes a first capacitor and a second capacitor, the first and second capacitors being connected together in

series.

15. The method of Claim 13, further comprising:

storing a bit of configuration information in a memory cell structure, the bit of configuration information determining which of the plurality of data input leads is the selected data input lead.

16. The method of Claim 13, further comprising:

biasing the intervening node with a bias voltage such that the intervening node is biased at the bias voltage immediately prior to the signal edge of the first digital signal being coupled onto the intervening node.

17. The method of Claim 13, wherein the first and second digital signals are signals propagating in an programmable interconnect structure of a field programmable gate array.

18. The method of Claim 17, further comprising:

supplying the digital output signal to an input lead of a block of configurable logic, the block of configurable logic being a part of the field programmable gate array.

19. The method of Claim 13, wherein the plurality of series capacitor coupling (SCC) structures that capacitively couples the selected data input lead to the intervening node is a multi-stage tree of SCC structures.

20. A multiplexer having a plurality of data input leads and a data output lead, the multiplexer comprising:

means for capacitively coupling a selected one of the plurality of data input leads to an intermediate node; and

an output latch having an input lead and an output lead, the input lead being coupled to the intermediate node, the output lead being coupled to the data output lead of the multiplexer.

21. The multiplexer of Claim 20, wherein the means comprises at least one memory cell that stores at least one bit of configuration information, the configuration information determining which of the plurality of data input leads is the selected data input lead.